REMARKS

On 06/23/2003, submitted the attached Power of Attorney and receipt card. The Power of Attorney seems to have been entered, as Applicant's representative is able to access the case on Private PAIR. However, PAIR does not show the customer number of 26384. The present office action was mailed to the previous attorney. Applicant requests that the correspondence address be updated to customer number 26384. Applicant also requests that the docket number of this case be changed to NC 84,832.

Claims 1-30 are pending in the application. No claims are presently allowed.

Claims 1, 11, and 21 are amended to recite that the shifter shifts according to an offset parameter (supported by paragraph 0033, lines 3-5), and generates a shifted operand (0033, lines 8-10) and a shift carry operand (0042, lines 4-7), and that the register stores the shift carry operand (0034, line 1). These claims are also amended to incorporate the limitation of claims 2, 12, and 22 regarding decoding the offset parameter into a mask field.

Claims 2, 12, and 22 are amended to cancel the limitation incorporated into claims 1, 11, an 21, and to add the word "further" for clarity.

Claims 2 and 22 are amended to change "at least a bit formatter" to "at least one bit formatter" for clarity.

Specification

The abstract was objected to for not reflecting the inventive feature of the invention. An amended abstract, with and without markings is attached. The amended abstract recites the decoder.

Claim Rejections – 35 U.S.C. § 112

Claims 1-30 have been rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Specifically, claims 1, 11, and 21 were rejected for lack of clarity regarding the difference between the shifted operand and shift carry operand and regarding the use of the shift carry operand. The claims have been amended to recite that both the shifted operand and shift carry operand are generated by the shifter. Both are fed into the shift post processor, as shown in Fig. 3. The first use of the shift carry operand is to be stored in the register. Dependent claims 6,

9, 16, 19, 26, and 29 recite further uses of the shift carry operand.

These claims were also rejected for lack of clarity of the processing done on the shifted operand. This is explained by the limitation regarding the use of a decoder and a mask field, incorporated from claims 2, 12, and 22. The processing of each bit depends partly on the corresponding bit of the field mask. Fig. 8 shows an example of one kind of processing that may be done.

These claims were also rejected for lack of clarity of the origin and use of the offset parameter. The amended claims clarify that the offset parameter is an input into the process, and is used in shifting and in generating the field mask.

Claim Rejections – 35 U.S.C. § 102

Claims 1, 2, 11, 12, 21, 22 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Groves, US 5,222,225.

Groves discloses a method and system of manipulating a contiguous variable length sequence of data. The method can manipulate and shift individual bytes within words. The method uses masks having as many bits are there are bytes in a word. Each bit of a mask indicates how a byte should be processed (col. 4, lines 63-68).

The invention of claim 1, as amended, is an apparatus comprising: a shifter to shift an operand, a register, and a shift post processor. The shift post processor comprises a decoder to decode an offset parameter into a mask field, the mask field having a plurality of mask bits, each of the mask bits defining a bit position of the shifted operand to be operated on.

The Examiner stated (regarding claim 2 as filed) that the mask field of the present claims is taught by the Load Byte Merge Mask of Groves. However, the merge mask contains one bit for each byte of operand (col. 4, lines 63-68). A number of other disclosed masks also share this characteristic. However, the field mask of the present invention has one bit for each bit of the shifted operand. This allows for shifting by any number of bits, rather than only by whole bytes as in Groves.

Claims 11 and 21 are to a method and processing unit have all the limitations of claim 1 and are asserted to distinguish from the reference in the same manner as claim 1. Claims 2, 12, and 22 depend from and contain all the limitations of claims 1, 11, and 21 respectively and are asserted to distinguish from the reference in the same manner as claims 1, 11, and 21.

Serial No.: 09/933,786

PATENT APPLICATION
Docket No.: NC 84,832

In view of the foregoing, it is submitted that the application is now in condition for allowance.

In the event that a fee is required, please charge the fee to Deposit Account No. 50-0281, and in the event that there is a credit due, please credit Deposit Account No. 50-0281.

Respectfully submitted,

Joseph T. Grunkemeyer
Reg. No. 46,746
Phone No. 202-404-1556
Office of the Associate Counsel
(Patents), Code 1008.2
Naval Research Laboratory
4555 Overlook Ave, SW
Washington, DC 20375-5325